IN THE CLAIMS:

Please substitute the following claims for the same-numbered claims in the application:

1. (Currently Amended) A structure comprising:

a substrate;

a buried isolation layer over said substrate;

a fin field effect transistor (FinFET) over said buried isolation layer; and

a field effect transistor (FET) in said substrate, wherein an upper surface of a gate region of said FET is planar to an upper surface of a gate region of said FinFET.

2. (Original) The structure of claim 1, further comprising retrograde well regions in said substrate.

3. (Original) The structure of claim 1, wherein said FinFET comprises:

a semiconductor layer comprising sidewalls;

a first dielectric layer over said semiconductor layer;

a second dielectric layer along each of said sidewalls of said semiconductor layer;

the FinFET gate region over the first and second dielectric layers; and

FinFET source/drain regions on opposite sides of said FinFET gate region.

4. (Original) The structure of claim 1, wherein said FET comprises:

FET source/drain regions on opposite sides of the FET gate region; and

a gate dielectric layer between said FET gate region and said substrate.

5. (Original) The structure of claim 1, further comprising a shallow trench isolation region in said substrate.

6. (Currently Amended) A structure comprising:

a silicon-on-insulator (SOI) wafer comprising:

a substrate;

a buried insulator layer over said substrate; and

a semiconductor layer over said buried insulator layer;

a fin field effect transistor (FinFET) over said buried insulator layer; and

a field effect transistor (FET) integrated in said substrate, wherein an upper surface of a gate region of said FET is planar to an upper surface of a gate region of said FinFET.

7. (Original) The structure of claim 6, further comprising retrograde well regions in said substrate.

8. (Original) The structure of claim 6, wherein said FinFET comprises:

sidewalls on said semiconductor layer;

a first FinFET dielectric layer over said semiconductor layer;

a second FinFET dielectric layer along each of said sidewalls of said semiconductor layer;

the FinFET gate region over the first and second FinFET dielectric layers; and

FinFET source/drain regions on opposite sides of said FinFET gate region.

9. (Original) The structure of claim 6, wherein said FET comprises:

FET source/drain regions on opposite sides of the FET gate region; and

a gate dielectric layer between said FET gate region and said substrate.

10. (Original) The structure of claim 6, wherein said buried insulator layer comprises buried oxide.

11. (Original) The structure of claim 6, further comprising a shallow trench isolation region in said substrate.

12-20. (Canceled).

Please add the following new claims:

21. (New) A structure comprising:

a substrate;

a buried isolation layer over said substrate;

a fin field effect transistor (FinFET) over said buried isolation layer, said FinFET comprising a FinFET gate region having an upper surface; and

a field effect transistor (FET) in said substrate, said FET comprising a FET gate region having an upper surface,

wherein said upper surface of said FinFET gate region and said upper surface of said FET

gate region are at a same level.

22. (New) The structure of claim 21, further comprising retrograde well regions in said substrate.

23. (New) The structure of claim 21, wherein said FinFET comprises:

a semiconductor layer comprising sidewalls;

a first dielectric layer over said semiconductor layer;

a second dielectric layer along each of said sidewalls of said semiconductor layer;

said FinFET gate region over the first and second dielectric layers; and

FinFET source/drain regions on opposite sides of said FinFET gate region.

24. (New) The structure of claim 21, wherein said FET comprises:

FET source/drain regions on opposite sides of said FET gate region; and

a gate dielectric layer between said FET gate region and said substrate.

25. (New) The structure of claim 21, further comprising a shallow trench isolation region in said substrate.

26. (New) The structure of claim 1, wherein the FinFET gate region comprises a first overall height, wherein the FET gate region comprises a second overall height, and wherein said second overall height is greater than said first overall height.

27. (New) The structure of claim 6, wherein the FinFET gate region comprises a first overall height, wherein the FET gate region comprises a second overall height, and wherein said second overall height is greater than said first overall height.

28. (New) The structure of claim 21, wherein said FinFET gate region comprises a first overall height, wherein said FET gate region comprises a second overall height, and wherein said second overall height is greater than said first overall height.